

ABSTRACT OF THE DISCLOSURE

A testing architecture for a semiconductor memory device is described. The testing architecture comprises a microprocessor, as well as a result sorting and display device. When a start signal is received by the microprocessor, a clock signal is output from the microprocessor to the semiconductor memory device so that a data storing signal is output from the memory device to the microprocessor. When the data storing signal is received by the microprocessor, the data storing signal is tested and compared, and a testing result signal is output. The resorting and display device is used to output the start signal to the microprocessor, receive the result signal, and sort the result signal so as to display whether data stored by the semiconductor memory device is correct.

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